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NGUYEN, DONGHAI D

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 10/040,745
Filing Date: January 07, 2002
Appellant(s): KRESGE ET AL.

Jack P. Friedman
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on October 23, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

None

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 81, 88, 89, 90, and 92 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

4,882,454	Peterson et al	11-1989
5,691,041	Frankeny et al	11-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 80, 82-87, 91, 92-97 stand rejected under 35 U.S.C. 102(b) as being anticipated by US patent 4,882,454 to Peterson et al.

Regarding claim 80, Peterson et al. disclose a method of making a multi-layer interconnect structure, the method comprising: providing a thermally conductive layer (102) including first and second opposing surfaces (top and bottom surfaces of layer 102, as shown on Fig. 2); positioning first (310 in fig. 4 and it is equivalent to dielectric layer 101 in fig. 1 or insulating layer 201 in figs. 2-3) and second (311 in fig. 4 and it is equivalent to dielectric layer 101 in fig. 1 or insulating layer 202 in figs. 2-3) dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively; and positioning first (312 in fig. 4 and it is equivalent to conductive layer 105 in fig. 1) and second (313 in fig. 4 and it is equivalent to conductive layer 105 in fig. 1) pluralities of electrically conductive members on the first and second dielectric layers, each of said first and second pluralities of electrically

conductive members adapted for having solder connections (103/104; Col. 2, lines 2 and 18 disclose that the electrically conductive members capable of and are used for soldering connections) thereon, and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53).

Regarding claims 82 and 93, Peterson et al. disclose laminating a copper foil (105) onto the first and second dielectric layers (101); etching (Col. 2, lines 19-21) selected portion of copper foils to produce first and second pluralities of electrical conductive members (312, 313 in Fig. 4).

Regarding claims 83 and 94, Fig. 1 shows a third dielectric layer (second dielectric layer 101 above layer 102) on said the first dielectric layer (first dielectric layer 101 above layer 102) and on the first plurality of electrical conductive members (second conductive layer 105 above layer 102); removing portion of said third dielectric layer to expose portions of said first plurality of electrically conductive members (col. 3, lines 45-50); and forming a plurality of microvias (second blind via on top of layer 102) within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

In regard to claims 85 and 96, Fig. 1 shows a fourth dielectric layer (second dielectric layer 101 below layer 102) on said the second dielectric layer (first dielectric layer 101 below layer 102) and on the second plurality of electrical conductive members (second conductive layer 105 below layer 102); removing portion of said fourth dielectric layer to expose portions of said first plurality of electrically conductive members (col. 3, lines 45-50); and forming a plurality of microvias (second blind via on below of layer 102) within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

Regarding claims 84, 86, 95, and 97, the portions of third and fourth dielectric layers are removed by laser ablating (Col. 3, line 26).

Regarding claim 87, Peterson et al. disclose a method of making an electronic package comprising the steps of: providing a semiconductor chip (IC packaging, Col. 2, lines 2-3) having a first surface including a plurality of contact sites thereon (an integrated circuit must have a contact sites for electrically connect to the printed circuit board or interposer); providing a multi-layered interconnect structure (Fig. 1) including a thermally conducive layer (102), a first (310) and second (311) dielectric layers on the thermally conductive layer, and a first (312) and second (313) pluralities of electrically conductive members on the first and second dielectric layers; providing a first plurality of solder connections (103/104) on the first plurality of electrically conductive members; and connecting the first plurality of electrically conductive to plurality of contact sites on the chip (Col. 2, lines 1-3), and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53).

Regarding claim 91, Peterson et al. disclose a method of making a multi-layer interconnect structure, the method comprising: providing a thermally conductive layer (102); positioning first (310 in fig. 4 or second dielectric layer 101 on top of layer 102 in fig. 1) and second (311 in fig. 4 or second dielectric layer 101 on bottom of layer 102 in fig. 1) dielectric layers on the thermally conductive layer; positioning first electrically conductive layer (312 in fig. 4 or second conductive layer 105 on top of layer 102 in fig. 1) within the first dielectric layer; positioning a second electrically conductive layer (302 in fig. 2 or first conductive layer 105 above layer 102 in fig. 1) between said first electrically conductive layer (second "conductive layer 105" counting up from the layer 102 in fig. 1 or conductive layer 312 in fig. 4)

and said thermally conductive layer (102) wherein said second electrically conductive layer comprising a first plurality of shielded signal conductors (302/105); and position first (105) and second (105) pluralities of electrically conductive members (Fig. 1) on the first and second dielectric layers (101), each of said first and second pluralities of electrically conductive members adapted for having solder connections (103 and 104) thereon, and the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 40-53).

Claims 81, 88, and 92 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al.

Regarding claims 81 and 92, Peterson et al. disclose the step of laminating except for the specific range of temperature and pressure. At the time the invention was made it would have been obvious matter of design choice to one having ordinary skill in the art to specify a specific range of temperature and pressure in the step of lamination because Applicants have not disclosed that the specific temperature and pressure provide an advantage, are used for a particular purpose, or solve a stated problem. One ordinary skill in the art would have expected claimed inventions to perform equally well as Peterson et al's invention. Therefore, it would have been obvious matter of design choice to specify a specific range of temperature and pressure in the step of laminating the first and second dielectric layers onto the thermally conductive layer to obtain the invention as specified in claims 81 and 92.

Regarding claim 88, Peterson et al. disclose forming a plurality of open in third dielectric layer (second dielectric layer 101 in Fig. 1) that exposing a portion of the first plurality of

electrically conductive members; plating a conductive layer to form a plurality of microvias (106, 107 and col. 3, lines 50-51; etc.) and using solder connections to connect printed wiring board to the mounting components, but Peterson et al. do not disclose specific steps of applying and re-flowing a first solder paste. It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply and re-flow a first solder paste onto the conductive layer since it is a conventional method of attaching surface mounting components to the wiring board using soldering.

Claims 89 and 90 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson et al in view of US Patent 5,691,041 to Frankeny et al.

Regarding claim 89, Peterson et al. disclose the claim invention except for applying a second solder paste on solder connections, positioning the contact member on a semiconductor chip against solder connections, and reflowing second solder paste to electrically connect said semiconductor chip to the multi-layer interconnect structure. However, Frankeny et al. disclose the steps applying a second solder paste on solder connections; positioning the contact members on the semiconductor chip against solder connections, and reflowing second solder paste to electrically connect said semiconductor chip to the multi-layer interconnect structure (Fig. 6 and Col. 1, lines 43-50) for improving and sealing the electrical connections (Col. 5, lines 13-14). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Peterson to have the steps of applying a second solder paste on solder connections; positioning the contact members on the semiconductor chip against the solder connection, and reflowing second solder paste as taught by Frankeny et al. for improving and

sealing the electrically connections between said semiconductor chip to the multi-layer interconnect structure.

Regarding claim 90, Peterson et al. disclose the step of proving a second plurality of solder connections (104) for connect to surface mounting device, except connecting second plurality of solder connections to the connecting pads of the circuitized substrate; however, Frankeny et al. shows a circuitized substrate (10) connecting with second plurality of solder connections (9 in Fig. 6) for mounting the interposer, "multi-layer structure" to the circuit board. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Peterson et al to have the step of connecting second plurality of solder connections to the connecting pads of the circuitized substrate as taught by Frankeny et al for mounting a multi-layer structure to the printed circuit board.

(11) Response to Argument

ISSUE 1:

Regarding claims 80, 87, and 91, Appellants argue in the appeal brief that Peterson does not disclose "positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate".

Examiner disagrees because Peterson discloses the step of positioning first (312 in fig. 4 and it is equivalent to "conductive layer 105" in fig. 1) and second (313 in fig. 4 and it is

equivalent to "conductive layer 105" in fig. 1) pluralities of electrically conductive members on said first (310 in fig. 4 and it is equivalent to "dielectric layer 101" in fig. 1 or "insulating layer 201" in figs. 2-3) and second (311 and it is equivalent to 101 in fig. 1 or 202 in figs. 2-3) dielectric layers, respectively, each of said first and second pluralities of said conductive members adapted for having solder connections (103 and 104; Col. 2, lines 2 and 18 disclose that the electrically conductive members capable of and are used for soldering connections) thereon for being electrically connected to a semiconductor chip and a circuitized substrate (col. 1, lines 15-16 disclose the IC packaging, "Semiconductor chip" and Col. 3, lines 61-68 disclose that Peterson's invention capable of interconnecting between two opposing surfaces, "semiconductor and circuitized substrate".

In addition, a recitation of the intended use of the claimed invention, the first and second pluralities of said conductive members "adapted for having solder connections" and solder connections "for being electrically connected to a semiconductor chip and a circuitized substrate", must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Peterson has the structure, first and second pluralities of the conductive members (312 and 313 in fig. 4 and they are equivalent to the second conductive layer 105 on top and bottom of layer 102 in fig. 1), and solder connection (103/104), is capable of performing the intended use (Col. 2, lines 2 and 18), therefore, it meets the claim.

Furthermore, Appellants have not positively claimed the step of electrically connecting/mounting the semiconductor chip and a circuitized substrate to the electrically conductive members as well as the step of having the solder connections on the electrically conductive members.

Also in claims 80, 87, and 91, Appellants argue that Peterson does not teach "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate". The Examiner disagrees since Col. 2, lines 40-53 of Peterson disclose the thermally conductive layer is optimized by proper choice of material, "coefficient of thermal expansion", and geometries, "selected thickness", to prevent the mismatch thermal expansion characteristics between printed wiring board and mounting devices (Col 1, lines 34-44). The mismatch thermal expansion characteristics between printed wiring board and mounting devices causes the solder connections between printed wiring board and mounting devices to fail. Therefore, preventing the mismatch of thermal expansion will prevent the failure of solder connections.

Appellants state that Peterson's disclosure is "non-specific" in col. 2, lines 44-49. However, Col. 2, lines 50-51 clearly states "These" (core modifications which are CTE and geometries, "thickness") involve the use of the materials or composite to made up the core. Therefore it is clearly or inherently identify the geometry and materials of the core, "thermally

conductive layer" is to be controlled. Furthermore, there is no positively statement in Peterson that precludes the geometries, "thickness" of the core from being modified.

Examiner acknowledges that in Col. 2, lines 13-19 of Peterson disclose another advantage of his invention for having the elongated pads have a spring action that reduces the stress on the solder connections. As stated in Col. 1, lines 30-39, there are at least two methods to reduce mismatch between printed wiring and mounting components. One of the objects of Peterson's inventions is to have the printed wiring board, "multi-layer interconnection structure" that has the similar thermal expansion characteristics as mounting components, "semiconductor chip and circuitized substrate" and the other is the deflection of the printed wiring board. Therefore, optimizing the core by proper choice of material and geometries to have the similar thermal expansion as mounting components to promote reliability of solder connections is an invention of Peterson.

Appellants' argument that Peterson does not teach a semiconductor chip and solder connections adapted to be connected to a semiconductor chip, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure (IC packaging, "semiconductor chip", in col. 1, lines 15-16; mounting pad, "solder connection", 103/104) is capable of performing the intended use (col. 2, lines 2-3), then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Appellants argue that Peterson does not teach the step of "positioning a second electrically conductive layer between said first electrically conductive layer and said thermally conductive layer wherein said second electrically conductive layer comprising a first plurality of shielded signal conductors" in claim 91.

Examiner disagrees because Peterson clearly discloses the first plurality shielded signal conductors (302 in fig. 2 or first conductive layer 105 on top of layer 102 in fig. 1) are the same as the second conductive layer, and they are shielded by the first conductor (312 in fig.4 or second conductive layer 105 on top of layer 102 in fig. 1) and the thermally conductive layer (102).

ISSUE 2:

Regarding claims 81 and 92, Appellants argue that the Examiner has not demonstrated that one having ordinary skill in the art would laminate the first and second dielectric layers onto the thermally conductive layer at pressure of from about 1000 to 1500 psi and at a temperature of from 600 to about 750 degrees Celsius. Peterson's col. 2, lines 62-63 disclose the first and second dielectric layers laminates onto the thermally conductive layer. This laminating step to form the printed circuit board is must perform at certain range of pressure and temperature, which may include the pressure and temperature range disclosed by Appellants or other pressure and temperature ranges. There is no limitation in the claim or specification that precludes the use different pressure and temperature in the process of laminating the first and second dielectric layer onto the thermally conductive layer.

Regarding claim 88, Appellants argue that Examiner has not established a *prima facie* case of obviousness. The Examiner disagrees because Peterson discloses the use of soldering to connect printed circuit board to mounting components (Col. 2, line 18), except the specific steps of how the solder connections are formed. However, it is well know in the art that when mounting a component to the printed circuit board by soldering, the soldering material is applying and re-flowing to attach the mounting component to the printed circuit board.

ISSUE: 3

Regarding claim 89, Appellants argue that The Examiner has not established a *prima facie* case of obviousness. The Examiner directs attention to Col. 1, lines 3-50 of Frankeny, which discloses the step of electrically connecting a semiconductor chip to the printed circuit board by solder re-flowed method is conventional.

Regarding claim 90, Appellants argue that one of ordinary skill in the art at the time the invention was made was not aware of the claimed invention. Frankeny discloses the claimed inventive step before November 25, 1997 that is long before Appellants' claimed invention. Also Frankeny discloses the step of connecting circuit board (10) to the solder connections (9) of the interposer (3), "multiplayer interconnect structure" for testing and replacement purposes (Frankeny's Abstract).

Last but not least, in all the claims, Appellants have not positively claimed the step of connecting the semiconductor chip and circuitized substrate to the multi-layer structure. All Appellants have claimed that the multi-layer structure adapted for (or for being) electrically connected a semiconductor chip and a circuitized substrate. Peterson's Col. 1, lines 30-40 disclose Peterson's printed wiring board capable of, "adapted for", connecting surface-mounting devices, i.e. semiconductor chip and circuitized substrate. If Appellants had positively claimed the step of electrically connecting the semiconductor chip and circuitized substrate to the multi-layer structure, then a rejection under 35 U.S.C. 103(a) comprising Peterson in view of Frankeny (as Prior Art of record), would have been made in stead of the 35 U.S.C. 102(b) rejection.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

DN
December 12, 2003

Conferees

Allen Shoap, SPE of AU 3723

Peter Vo, SPE of AU 3726/3729

PETER VO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3700

IBM Corporation / IP Law N50/040-4
1701 North Street
Endicott, NY 13760